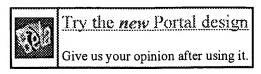


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Tiny instruction caches for low power embedded systems

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Ann Gordon-Ross , Susan Cotterell , Frank Vahid

ACM Transactions on Embedded Computing Systems (TECS) November 2003 Volume 2 Issue 4

Instruction caches have traditionally been used to improve software performance. Recently, several tiny instruction cache designs, including filter caches and dynamic loop caches, have been proposed to instead reduce software power. We propose several new tiny instruction cache designs, including preloaded loop caches, and onelevel and two-level hybrid dynamic/preloaded loop caches. We evaluate the existing and proposed designs on embedded system software benchmarks from both the Powerstone and ...

2 Hardware implementation of loop trace and microprogram synthesis A. M. ADB-Alla , Laird H. Moffett

100%

Proceedings of the 1975 annual conference January 1975

The modification or tuning of the microcode in a computer that utilizes a writable control store is one method whereby a program's execution time can be improved. A method for automatically performing a microcode tuning or synthesis has been developed by Drs. Karlgaard and Abd-alla and is discussed in detail in [1]. Presented is an extension of this effort which allows microcode synthesis to be performed "onthe-fly". This is accomplished by: (1) performing the required program ...

On-line architecture tuning using microcapture

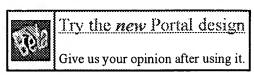
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A. M. Abd-Alla , Laird H. Moffett

ACM SIGARCH Computer Architecture News, Proceedings of the 3rd annual symposium on Computer architecture January 1976 Volume 4 Issue 4



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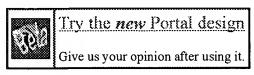
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Session 6: Log write-ahead protocols and IMS/VS logging R. J. Peterson , J. P. Strickland Proceedings of the 2nd ACM SIGACT-SIGMOD symposium on Principle database systems March 1983	100% es of
Purely functional, real-time deques with catenation Haim Kaplan , Robert E. Tarjan Journal of the ACM (JACM) September 1999 Volume 46 Issue 5 We describe an efficient, purely functional implementation of deques with In addition to being an intriguing problem in its own right, finding a purel implementation of catenable deques is required to add certain sophisticat programming constructs to functional programming languages. Our solut worst-case running time of O(1) for each push, pop, inject, eject and cate best previously known solution has an O(log	ly functional ted ion has a
3 Literate programming Christopher J. Van Wyk Communications of the ACM December 1988 Volume 31 Issue 12	100%
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This is a tutorial introduction to assertional reasoning based on temporal logic. The

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Segment-based proxy caching of multimedia streams

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Kun-Lung Wu , Philip S. Yu , Joel L. Wolf

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Lixin Gao , Zhi-Li Zhang , Don Towsley

IEEE/ACM Transactions on Networking (TON) December 2003

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We present a proxy-assisted video delivery architecture that can simultaneously reduce the resources requirements at the central server and the service latency experienced by clients (i.e., end users). Under the proposed video delivery architecture, we develop and analyze two novel proxy-assisted video streaming techniques for on-demand delivery of video objects to a large number of clients. By taking advantage of the resources available at the proxy servers, these techniques not only significan ...

3 IPStash: a Power-Efficient Memory Architecture for IP-lookup Stefanos Kaxiras , Georgios Keramidas

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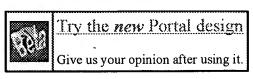
Proceedings of the 36th Annual IEEE/ACM International Symposium on

Microarchitecture December 2003

High-speed routers often use commodity, fully-associative,TCAMs (Ternary Content AddressableMemories) to perform packet classification and routing (IP-lookup). We propose a memory architecture calledIPStash to actasa TCAMreplacement, offering



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Performance issues of enterprise level web proxies

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Carlos Maltzahn , Kathy J. Richardson , Dirk Grunwald

ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems June 1997

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Enterprise level web proxies relay world-wide web traffic between private networks and the Internet. They improve security, save network bandwidth, and reduce network latency. While the performance of web proxies has been analyzed based on synthetic workloads, little is known about their performance on real workloads. In this paper we present a study of two web proxies (CERN and Squid) executing real workloads on Digital's Palo Alto Gateway. We demonstrate that the simple CERN proxy architecture ...

2 Session 9: hardware performance: Cache performance in vector 41 supercomputers

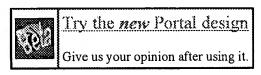
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L. I. Kontothanassis, R. A. Sugumar, G. J. Faanes, J. E. Smith, M. L. Scott Proceedings of the 1994 ACM/IEEE conference on Supercomputing November 1994

Traditional supercomputers use a flat multi-bank SRAM memory organization to supply high bandwidth at low latency. Most other computers use a hierarchical organization with a small SRAM cache and slower, cheaper DRAM for main memory. Such systems rely heavily on data locality for achieving optimum performance. This paper evaluates cache-based memory systems for vector supercomputers. We develop a simulation model for a cache-based version of the Cray Research C90 and use the NAS parallel



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4 OS-controlled cache predictability for real-time systems

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	3 Improving memory energy using access pattern classification Kandemir, M.; Sezer, U.; Delaluz, V.; Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Confe on , 4-8 Nov. 2001 Pages: 201 - 206	ere
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Kontothanassis, L.I.; Sugumar, R.A.; Faanes, G.J.; Smith, J.E.; Scott, M.L.; Supercomputing '94. Proceedings , 14-18 Nov. 1994 Pages: 255 - 264

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	3 Multilevel aligned IP prefix caching based on singleton information Woei-Luen Shyu; Cheng-Shong Wu; Ting-Chao Hou; Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume 3 , 17-21 Nov. 2002 Pages: 2345 - 2349 vol.3

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4 Reducing cache miss ratio for routing prefix cache

Huan Liu;

Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE , Volume 3 , 17-21 Nov. 2002

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